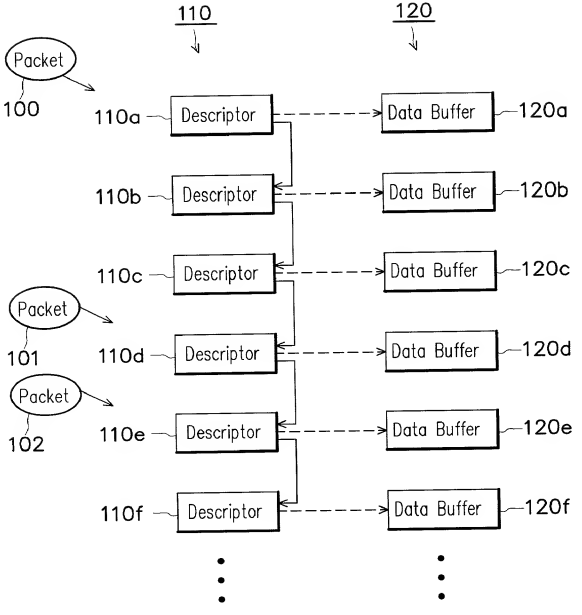

FIG. 1 (PRIOR ART)

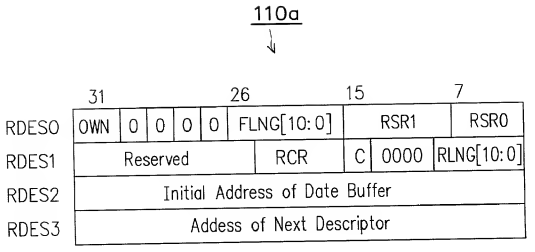
110a
31
26
15
7
RDES0
OWN
0
0
0
0
FLNG[10:0]
RSR1
RSR0
RDES1
Reserved
RCR
C
0000
RLNG[10:0]
RDES2
Initial Address of Date Buffer
RDES3
Addess of Next Descriptor

FIG. 2

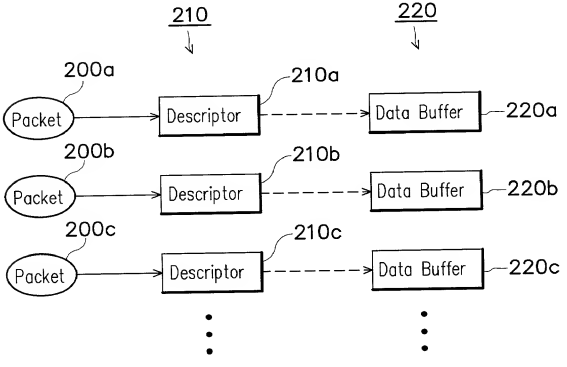
210
220
200a
210a
Packet
Descriptor
Data Buffer
220a
200b
210b
Packet
Descriptor
Data Buffer
220b
200c
210c
Packet
Descriptor
Data Buffer
220c

FIG. 3

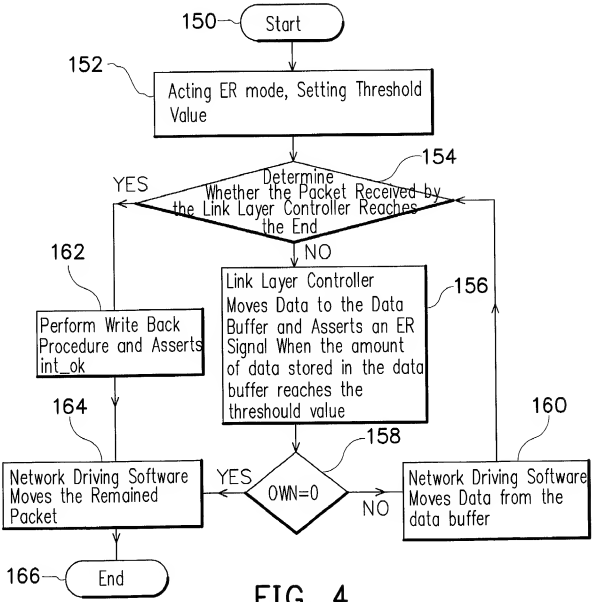

FIG. 4

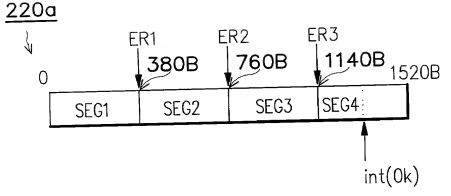

FIG. 5